Constructional Project

# FREQUENCY STANDARD GENERATOR

ANDY FLIND

*A high-precision selectable 1Hz to 100kHz frequency source derived from BBC Radio Four's transmission signal.*

DURING the design stage of the *Synchronous Clock Driver*, featured in *EPE* Sept '01, doubts arose as to the accuracy of the frequency meter being used to check and adjust the output frequency of the project. Since this instrument was the author's primary means of measuring frequency, the difficulty arose as to how it could itself be checked and, if necessary, adjusted.

## TRANSMISSION FREQUENCIES

One of the broadcast radio carrier signals appeared to be the best way of obtaining a suitable reference. Most British readers will know of the time signal transmitted at 60kHz from Rugby, but this isn't really suitable for frequency testing since it is pulsed on and off by the data signals it carries.

Another source which seemed better suited for the purpose was the 198kHz "longwave" carrier for *Radio 4*. Originally this was intended for use as a national frequency standard and its accuracy is still maintained to an incredible level, having a Rubidium frequency source as its reference with constant monitoring by the National Physical Laboratory.

In fact, the accuracy is claimed to be one part in $10^{11}$, which translates to about a third of a millisecond per year of error. This should be more than adequate as a standard for most home workshops!

## HOME SERVICE DESIGNING

Various circuits are available for receiving and using this signal "off air", so one was soon obtained through the good offices of one of our better radio magazines and hastily constructed. In fact, the "error" of the author's meter turned out to be of insignificant proportions, but by then the "design bug" had bitten.

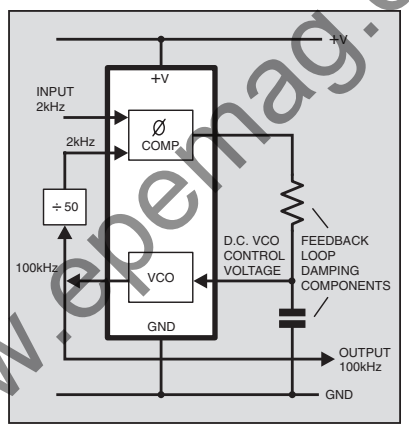



*Fig.1. Phase-locked loop principle.*

Could a better version be built offering more useful output frequencies such as 100kHz and the decades beneath it, 10kHz, 1kHz and so forth? Such a source would be very useful for calibrating all sorts of equipment, including oscilloscopes and frequency meters, and perhaps also in the testing and adjustment of clocks.

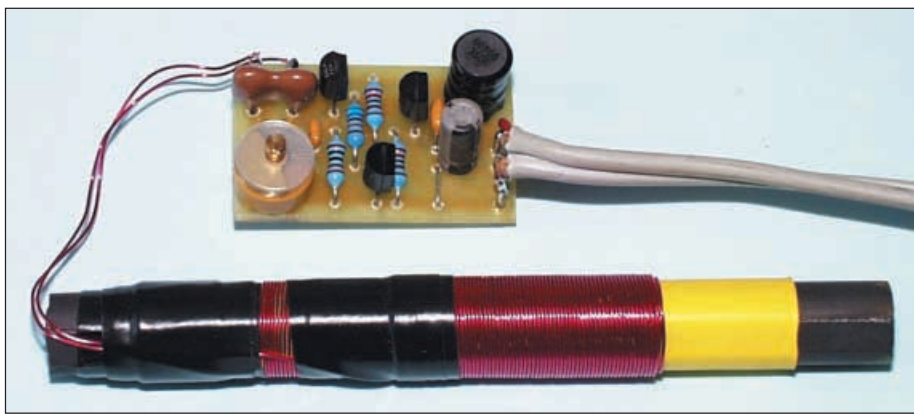
Electronic "old-timers" sometimes fondly recall the days when Radio 4 (the Home Service for really old-timers!) was broadcast on the longwave frequency of 200kHz. Division by two gave a perfect 100kHz squarewave and subsequent decade dividers could reduce this to any required value.

## FREQUENCY CHANGING

Nowadays, getting to 100kHz from 198kHz presents slightly more difficulty. It turns out that the largest factor common to both frequencies is just 2, so to obtain 100kHz one must divide by 99 and then multiply by 50, but not necessarily in that order. Division is easy enough using modern logic, even with an odd number like 99.

Multiplication requires a phase-locked loop (PLL), however, with a divider in the feedback circuit. How this method was used to obtain 100kHz from a 2kHz input is shown in Fig.1. The most important components of the phase-locked loop, a phase comparator and a voltage-controlled oscillator (VCO), are shown here.

In essence, the input is compared with a feedback signal from the voltage-controlled oscillator and if the two are not in phase the phase comparator adjusts a control voltage to bring the oscillator into line with the input. A couple of external components filter the control voltage to ensure stability.



If the output is divided by a discrete factor *n* before going to the comparator the oscillator will automatically run at *n* times the input frequency, so frequency multiplication is achieved. Integrated phase-locked loop devices are available with most of the necessary building blocks contained internally.

## PHASE-LOCKED LOOP

The CMOS 4046 phase-locked loop device has been around for some years and has many useful features, including a phase comparator that can operate happily with signals which do not have equal mark-space ratios, and a high impedance input for the VCO control voltage to simplify the loop filter design.

In the author's first attempt at this design, the 198kHz signal was divided by 99 to obtain 2kHz and then multiplied by 50 using a phase-locked loop. However, unlike dividing circuits these loops are inherently slightly unstable since the output frequency is controlled by a series of minute adjustments of the oscillator control voltage, made each time a phase comparison takes place.

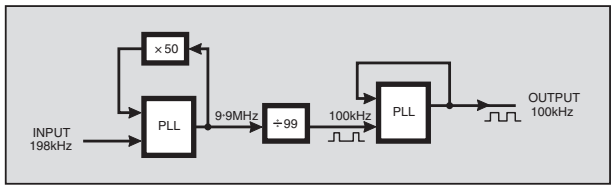



*Fig.2. Block diagram showing conversion from 198kHz to 100kHz.*

It follows that with an input of only 2kHz and an output of 100kHz the output frequency is only adjusted every 500$\mu$s, or fifty output cycles, allowing plenty of scope for output phase jitter and perhaps short-term frequency errors. It was decided therefore to try operating the circuit the other way round, with multiplication before division, as this would result in the adjustments taking place very nearly twice per cycle of output frequency.

The block diagram of this is shown in Fig.2, where the first PLL multiplies the 198kHz input to 9·9MHz, which is then divided by 99 to reach 100kHz. The divider circuit output has an uneven mark-space ratio so it is passed through a further PLL, this time without a divider, to produce the same frequency but as a perfect squarewave.

Whilst the intermediate frequency of 9·9MHz is well above the capability of ordinary CMOS, it is well within the range of *high-speed* CMOS devices (74HC series).

## RECEIVER CIRCUIT

Moving on to the circuit shown in Fig.3, this is the Receiver used to obtain the signal "off-air". A lot of difficulty was initially encountered due to feedback from later parts of the circuit, but as soon as the receiver circuit was positioned a metre or so away from the rest of the unit on screened leads these problems vanished.

The Receiver was therefore designed as a separate unit with its own small printed circuit board (p.c.b.). Coil L1 is wound on a short ferrite rod and uses fixed capacitor C1 with variable capacitor VC1 to tune it to


resonance at 198kHz. Field effect transistor (f.e.t.) TR1 buffers this resonant circuit to minimize loading whilst transistors TR2 and TR3 provide voltage gain and buffering of the output before the main circuit.

A regulated power supply of 5V is used as this can be taken from the supply for the following high-speed CMOS circuit. Connections are made with screened twin "figure-of-eight" audio lead, with the power arriving through one core, the output signal leaving through the other and the two screens acting as ground or 0V.

Local supply decoupling is provided by capacitors C3 and C4 with choke L2 in place of the usual resistor, since with a supply of only 5V the voltage drop across a resistor would be unacceptable. The output from this circuit obviously depends on the signal available, but at the author's location, some 100 miles from the Droitwich transmitter, it is about 400mV peak-to-peak.

The circuit also continued to operate well during a period of drastically reduced transmitter power over a maintenance period, suggesting that a much greater operating range is achievable.

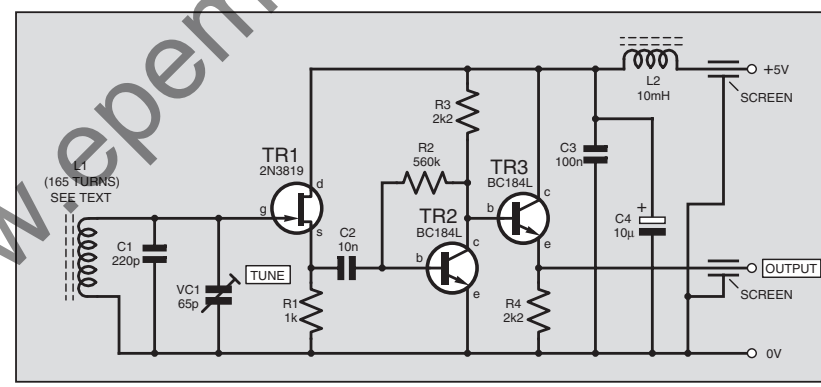



*Fig.3. Full circuit diagram for the Receiver section of the Frequency Standard Generator.*



## COMPONENTS

*Approx. Cost Guidance Only* **£6**

### Receiver

See SHOP TALK page

**Resistors**

| | |
|---|---|
| R1 | 1k |
| R2 | 560k |
| R3, R4 | 2k2 (2 off) |

All 0·6W 1% metal film

**Capacitors**

| | |
|---|---|
| C1 | 220p silvered mica |
| C2 | 10n resin-dipped ceramic |
| C3 | 100n resin-dipped ceramic |
| C4 | 10$\mu$ radial elect. 50V |
| VC1 | 5·5p to 65p trimmer |

**Semiconductors**

| | |
|---|---|
| TR1 | 2N3819 *n*-channel field effect transistor |
| TR2, TR3 | BC184L *npn* transistor (2 off) |

**Miscellaneous**

| | |
|---|---|
| L1 | ferrite rod, 10mm dia x 100mm length (see text), 165 turns 0·4mm enamelled copper wire |
| L2 | 10mH choke |

Printed circuit board (Receiver), available from the *EPE PCB Service,* code 353; plastic container, see text.

## MAIN CIRCUIT

In the main circuit of Fig.4 the signal is first amplified to logic levels. This amplifier was the main cause of feedback problems when the receiver was close to it, since it inevitably re-radiates a little of the amplified signal. After much trial and error, the simple amplifier based on IC1, a CMOS 4007 transistor pair plus inverter i.c., is used as a three-stage amplifier, was found to be by far the most effective.

Each of the first two stages has an a.c. input coupling capacitor (C1 and C2) and a resistor (R1 and R2) to bias it into analogue operation, whilst the third stage buffers the output.

Next IC2, a 74HCT7046 which is a high-speed version of the 4046 PLL, raises the frequency to 9·9MHz. To do this it has a divide-by-50 circuit in its logic feedback, provided by binary divider IC3 and one half of the dual quad-input AND gate IC4a, again high-speed types. The gate decodes three outputs from IC3 and when these reach the binary equivalent of 50 it pulses IC3's Reset pin.

Preset VR1 is used to set the VCO to the centre of its control voltage range at the normal operating frequency. The 9·9MHz output from IC2 pin 4 is divided by another high-speed binary divider IC5, used with IC4b to divide this time by 99, again by decoding the divider outputs and pulsing the Reset pin (2) of IC5.

Two outputs are available from this part of the circuit. The first is raw 198kHz from IC1, at socket SK1. The second is the 100kHz from IC5 at SK2, which may be useful for checking frequency counters although it does not have an even mark-space ratio. Both of these are 0V to 5V logic-level outputs.

## LOGIC LEVEL SHIFTING

The high-speed versions of CMOS *must* have a supply of 5V so this is supplied by the 5V positive 100mA regulator IC6, which also supplies the receiver.

For reasons which will be explained, most of the rest of the circuit (IC8 and beyond) operates from a 12V supply. Consequently, IC8 acts as a comparator to convert the 5V logic output of IC5 into a 12V logic output. IC8 is a CA3130 CMOS op.amp, which is fairly fast and has a rail-to-rail output.

The signal from this drives IC9, this time a standard 4046 CMOS PLL. The purpose is to convert the input to a perfect 50:50 squarewave output. Preset VR2 is used to set the optimum operating point for the VCO, and the output is taken to the first of six output buffers provided by IC15.

The signal from IC8 also goes to the first of the string of five decade dividers IC10 to IC14, giving a series of frequencies down to 1Hz. It doesn't matter that the input to IC10 is not a squarewave since the output will be anyway. All the outputs are buffered by the remaining five buffers of IC15.

The reason for the 12V supply can now be explained. IC15 does more than simply buffer the outputs, it is also capable of "voltage translation", meaning that its output signal "high" or positive level is determined by its supply voltage. If a suitable variable supply is provided for this i.c. its output can be adjusted from about 3V to 15V.

However, for this to work the input signal "high" voltage must be greater than half the maximum supply voltage, so it is necessary to raise the supply voltage from 5V used by the first part of the circuit to the 12V used by the rest. The 12V supply is provided by regulator IC7 and the variable supply is generated by IC16, an LM317 adjustable positive regulator controlled by panel-mounted potentiometer VR3 used as a variable resistor.

Pushbutton switch S2 is fitted for resetting all the counters simultaneously so that they can be synchronized to an external event if necessary. As a manual switch this is really only useful for synchronizing the final output which counts seconds, but some form of electronic switching could be added here if this feature is required for a particular application.

It works by pulling all the reset inputs high very briefly at the instant the line from S2 goes positive. Resistor R11 and capacitor C20 ensure that only one reset pulse takes place for each operation of S2, eliminating the effects of switch bounce.

Power for all three regulators comes from the centre-tapped transformer T1 and rectifier diodes D1 and D2, together with main supply decoupling capacitor C14. T1 is a 15V-0V-15V type which produces about 20V of unregulated output in this circuit.

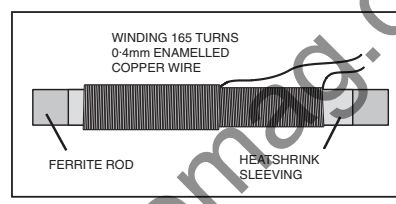



*Fig.5. Ferrite rod aerial winding details. Using 0·4mm enamelled copper wire and starting from one end, 100 turns are close-wound on the "sleeving" and then a further 65 turns are wound over this, working back towards the start, to give a total of 165 turns.*

## ANTENNA WINDING

Despite the apparent complexity of the circuit diagram, this is a relatively simple circuit to construct and test. It is suggested that the Receiver should be built and tested first as this is required for testing the remainder of the project.

The antenna is wound as shown in Fig.5 on a 10cm × 10mm diameter ferrite rod. The one obtained for the prototype had rather sharp lengthwise moulding edges so these were smoothed off with a file and a length of heat-shrink sleeving was fitted over it. Warming the ferrite a little before attempting to shrink the sleeve proved helpful for this process. The coil was then wound onto it using 0·4mm enamelled copper wire, which is relatively thick and easy to handle.

Starting about 10mm from one end, 100 turns were close-wound into position, then a further 65 turns were wound over this going back towards the start, giving a total of 165 turns altogether. The winding was secured with insulating tape, taking care to prevent the wire from coming into contact with the ferrite to avoid the possibility of insulation damage.

The tuning range of trimmer capacitor VC1 is quite small so if another type of rod

## COMPONENTS

### Digital Circuit

**Resistors**

| | |
|---|---|
| R1, R2 | 47k (2 off) |
| R3 | 15k |
| R4, R9 | 220k (2 off) |
| R5, R10 | 2k2 (2 off) |
| R6 | 39k |
| R7, R12 | 10k (2 off) |
| R8 | 100k |
| R11 | 470k |
| R13 | 470Ω |
| R14 | 560Ω |

All 0·6W 1% metal film

See SHOP TALK page

**Potentiometers**

| | |
|---|---|
| VR1 | 10k min. preset, horiz. |
| VR2 | 100k min. preset, horiz. |
| VR3 | 4k7 (or 5k) rotary carbon, lin. |

**Capacitors**

| | |
|---|---|
| C1, C2 | 10n resin-dipped ceramic (2 off) |
| C3, C21 | 100p ceramic (2 off) |
| C4 to C8, C10, C12, C13, C15, C16, C19, C20, C22, C24 | 100n resin-dipped ceramic (14 off) |
| C9, C11, C23 | 10μ radial elect. 50V (3 off) |
| C14 | 470μ radial elect. 35V |
| C17 | 470p ceramic |
| C18 | 470n resin-dipped ceramic |

**Semiconductors**

| | |
|---|---|
| D1, D2 | 1N4001 rec. diode (2 off) |
| IC1 | 4007UBE dual CMOS transistor pair/inverter |
| IC2 | 74HCT7046AE phase-locked loop |
| IC3, IC5 | 74HC4024 7-stage binary counter (2 off) |
| IC4 | 74HC21 dual quad-input AND gate |
| IC6 | 78L05 +5V 100mA voltage regulator |
| IC7 | 78L12 +12V 100mA voltage regulator |
| IC8 | CA3130E CMOS op.amp |
| IC9 | 4046 phase-locked loop |
| IC10 to IC14 | 4017B decade counter (5 off) |
| IC15 | 4050 hex buffer |
| IC16 | LM317 adjustable positive voltage regulator |

**Miscellaneous**

| | |
|---|---|
| S1 | d.p.s.t. mains switch |
| S2 | push-to-make switch |
| T1 | 15V-0V-15V 250mA mains transformer |

Printed circuit board (Digital), available from the *EPE PCB Service*, code 354; 8-pin d.i.l. socket; 14-pin d.i.l. socket (4 off); 16-pin d.i.l. sockets (8 off); 4mm chassis socket, red (8 off); 4mm chassis socket, black; metal case, see text; p.c.b. mounting supports, to suit; twin screened audio cable, see text; connecting wire; solder, etc.

***Approx. Cost Guidance Only*** **£25** ***excluding case***

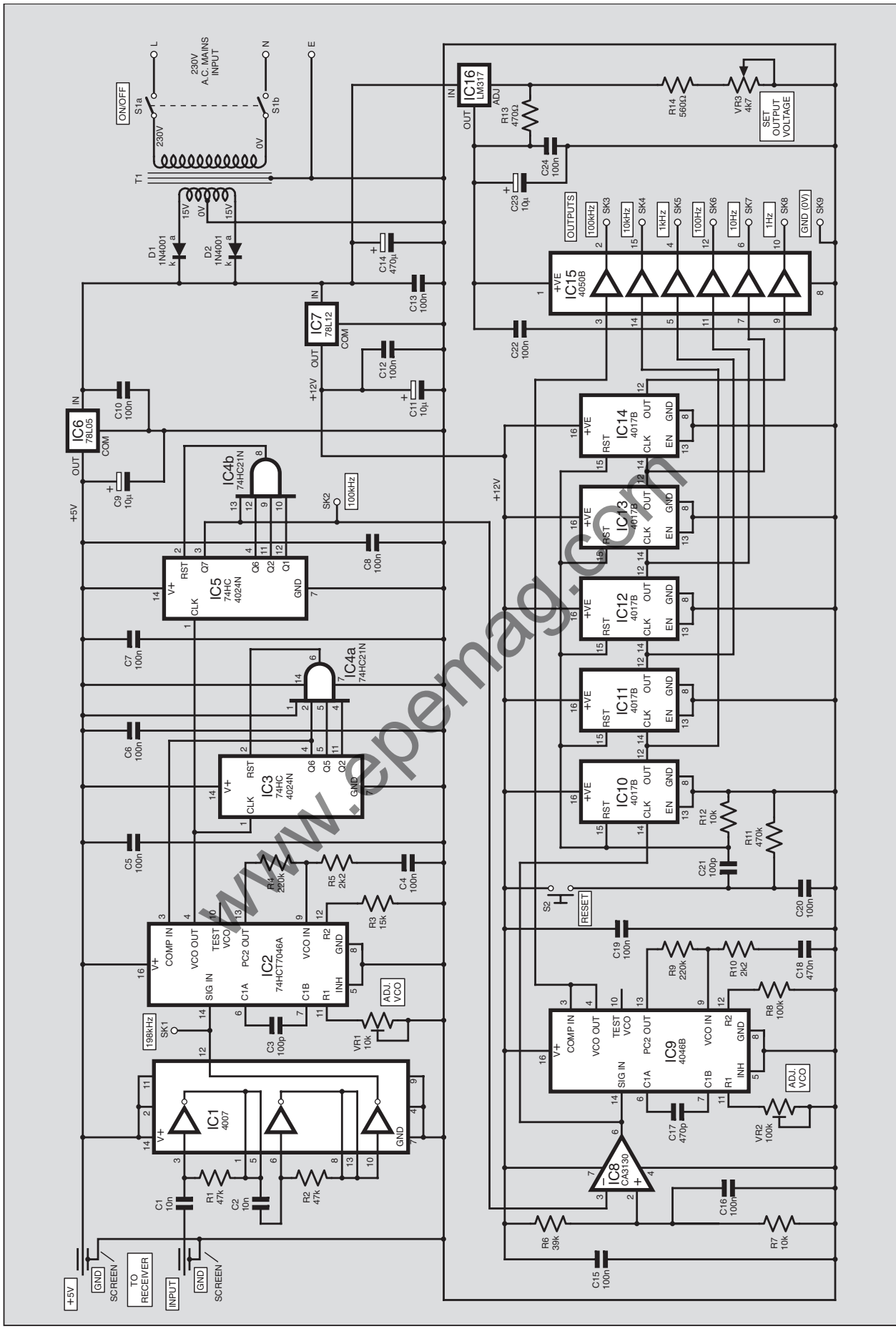
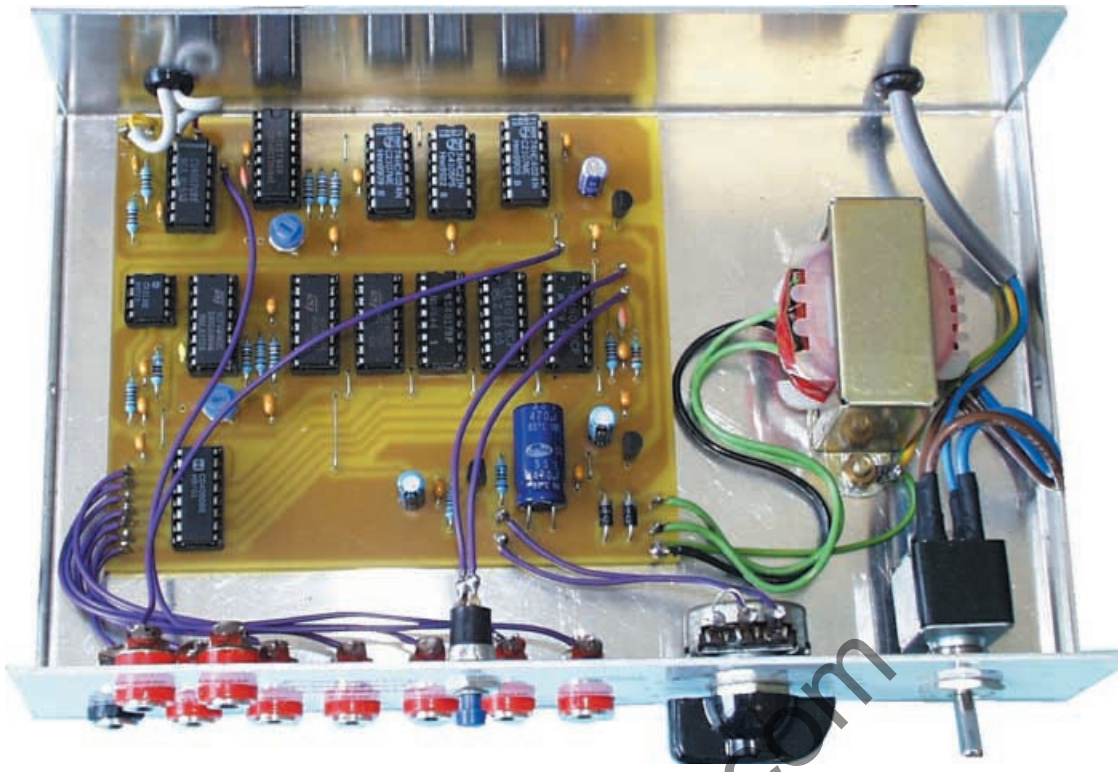





*Fig.4. Complete circuit diagram for the Digital section of the Frequency Standard Generator.*



is employed or difficulty is experienced in tuning a check of the resonant frequency may be needed. A simple method often used by the author is shown in Fig.6. It requires a frequency generator and an oscilloscope and is an extremely easy way to find the resonant frequency since the peak produced is quite unmistakable, much greater than those due to harmonics.

Turns can be simply added or removed on the coil until the desired point is reached.

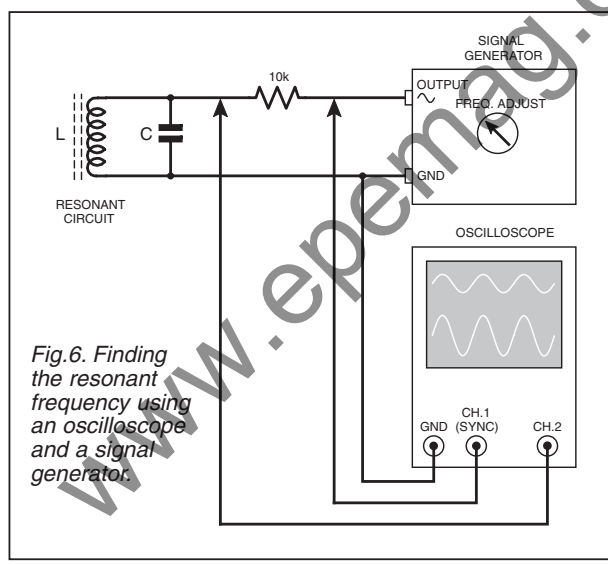



*Fig.6. Finding the resonant frequency using an oscilloscope and a signal generator.*

## RECEIVER CONSTRUCTION

The component layout of the Receiver p.c.b. is shown in Fig.7 and construction should present no problems. Note that capacitor C1 is a silvered-mica type for maximum stability. When powered at 5V with the antenna attached, it forms part of the biasing circuit and a small d.c. voltage should appear at the source (s) of TR1. The actual value of this voltage will depend on the characteristics of the individual f.e.t. used for TR1 but a figure of 0·5V to 2V should be acceptable.

Likewise, about 1·5V should be present at the emitter (e) of transistor TR3 though this will be dependent to some extent on the gain of TR2. A scope can be used to set the tuning, but if one is not available the test circuit shown in Fig.8 works well.

The diode drops about 0·5V so the output will be about 1V plus the peak value of the signal, so tuning should be adjusted for the maximum obtainable value. An analogue meter may be found preferable to a digital one when making this adjustment.

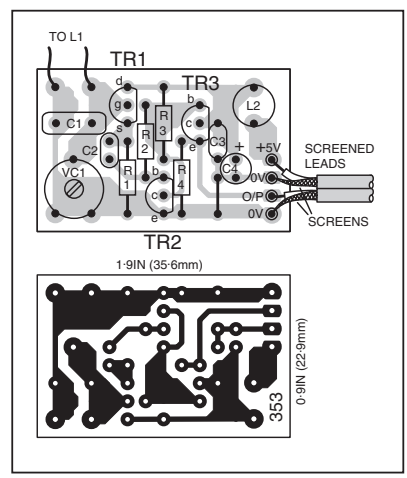



*Fig.7. Printed circuit board component layout, wiring and full-size copper foil master pattern for the Receiver.*

It should be remembered that the signal is amplitude modulated – a bit of a nuisance this, really! – so the level will fluctuate a little. Ferrite aerials are also very directional, so if difficulty is experienced in finding the signal it may be helpful to use a longwave radio receiver to find the correct orientation for it.

The receiver and aerial must be housed in a non-metallic case so that the radio signals can penetrate to them. The prototype uses the plastic tube from a pack of effervescent vitamin C tablets, which is about the right size and can easily be made waterproof. Small pieces of foam plastic secure the board and ferrite rod in place inside the tube.

Interconnection between Receiver and Digital board is made through "figure-of-8" twin screened audio cable. A couple of metres is all that is required, though in some areas of weak signal it may be preferable to place the receiver in an elevated or external location for reliable results.

## ASSEMBLY OPTIONS

If the full facilities of this project are not required it may not be necessary to construct all of it. For example, if a quick test of a frequency meter is all that is required, the Receiver on its own may be all that is

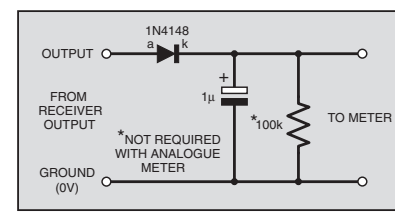



*Fig.8. Simple test circuit for tuning the Receiver.*

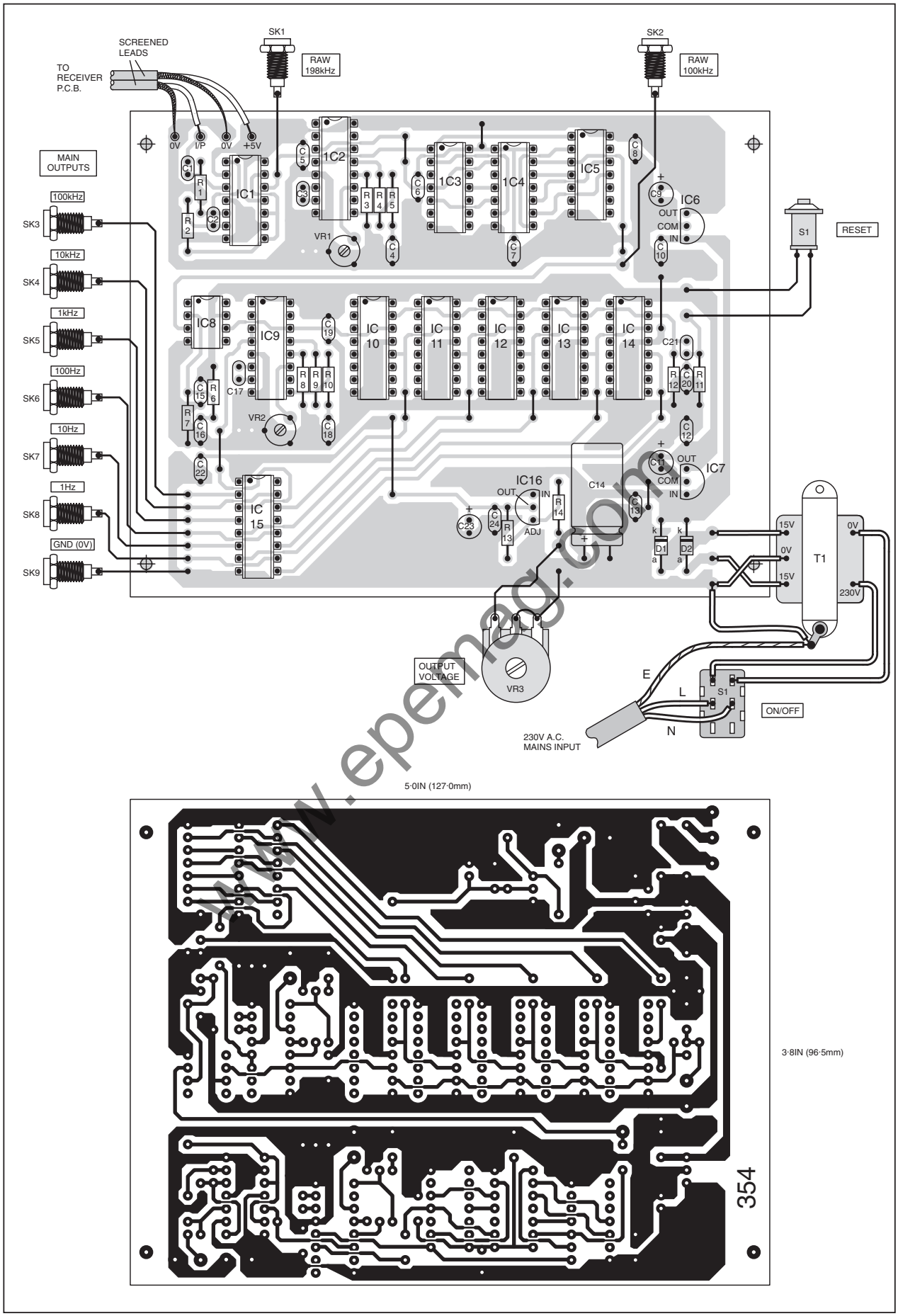





*Fig.9. Printed circuit board component layout, wiring and full-size master for the Digital board.*


needed. If the output level from this is insufficient, the amplifier section of IC1 of the main board and its associated components should be sufficient to do the job.

The p.c.b. component and track layout for the full digital circuit is shown in Fig.9. To simplify testing following construction, dual-in-line (d.i.l.) sockets are recommended for all the i.c.s, except, of course, for the three voltage regulators.

Where a current-limited bench power supply is available, use of this would be preferable to simply connecting the unit to its transformer and powering up. It can be connected across the leads of capacitor C14.

Construction should begin with the fitting of all the passive components, links, resistors, diodes and capacitors, then the d.i.l. sockets, then the 5V regulator IC6. The two presets VR1 and VR2 can also be fitted, holes are provided to accept a variety of types.

## TESTING

If the circuit is powered, with around 18V d.c. from a bench supply, the presence of the 5V regulated supply can be checked at the top right-hand pin of any of the upper five d.i.l. sockets. It should draw only a couple of milliamps from the supply at this stage.

If the receiver is connected and IC1 inserted into its socket, this should rise to about 5mA in total. The d.c. voltage at pin 12 of IC1 should measure as about 2·5V, indicating (hopefully!) that the output is operating at 198kHz squarewave. If a 'scope or frequency meter is available, these can be used to check it, of course.

Next, IC2, IC3, IC4 and IC5 can be inserted. These all work together so there is really no way of testing them individually. The method of setting up the operating point of IC2 is quite simple, a DVM should be connected between ground (negative) and pin 10 (Test VCO, positive) and VR1 carefully adjusted for a reading of about half the supply, or 2·5V.

The PLL should then be locked and working at the correct frequency and optimum VCO operating point. The output from IC5 pin 3 should now be exactly 100kHz, although it will not be a squarewave. A meter connected to it should read about 1·75V d.c. and a scope will show it as positive-going pulses. The overall supply drain should now be about 20mA.

Next the 12V regulator IC7 should be fitted and the presence of its output checked. This should appear at all of the positive supply pins for the logic i.c.s on the lower part of the board. The current drawn by IC7 should raise the supply current to about 23mA. If this checks out IC8 can be fitted, which will add another 1mA or so.

Following this the second PLL, IC9, can be fitted and adjusted in a similar manner to the first by monitoring the voltage at pin 10 whilst adjusting VR2. In this case, though, since the supply is 12V, the voltage set at this pin should be about 6V. The 100kHz squarewave output should now be available from pin 4 of IC9 and, of course, the average d.c. voltage measured here should be half the supply, or 6V. Total current consumption should now be about 25mA to 26mA.

After this the five 4017B decade dividers, IC10 to IC14, can be fitted. This made no perceptible difference to the supply current of the prototype. Their squarewave outputs, at pin 12, can be checked if required.

This leaves just the output buffer IC15 and its supply regulator to be fitted to complete the board. The variable regulator IC16 should be fitted first. With VR3 temporarily connected, the board should be powered again and the output from IC16 checked, pin 1 of the socket for IC15 can be used for this. Note that the pinout for IC15 is different from most CMOS devices in that, although pin 8 is negative, the positive supply is applied to pin 1. Rotating VR3 should cause this supply to vary between about 3V and 15V. If this works, IC15 can be inserted and its outputs checked.

## ENCLOSURE

Having completed the main board, it can now be fitted into the case of the constructor's choice and connected to the output sockets and the transformer as shown in Fig.9. A metal case is recommended, connected to mains earth as shown through a solder tag under one of the mounting bolts of transformer T1. This connection is essential as the high frequencies around IC2 to IC5, plus the squarewave nature of the signals throughout the circuit, can radiate some interference. Use of an earthed metal case does much to reduce this.

The outputs from this circuit can be used for many purposes, including the testing of digital circuits where the ability to vary their input signal voltage and use several outputs simultaneously should come in very useful (but do not exceed the power line voltage of the i.c.s. under test).

However, the primary virtue of this design is its phenomenal accuracy and stability. There will not usually be many really accurate standards of any kind in the workshop of a home constructor since they are usually prohibitively expensive. This design provides an exception to this rule by bringing a national frequency standard right onto the amateur's bench.

It should prove useful for checking and adjusting the calibration of frequency meters, oscilloscopes, and any other equipment used for measuring or generating frequency of any kind. □